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10/534,343	07/18/2005	Anthony Spencer	0120-032	4839
42015 7590 08/06/2009 POTOMAC PATENT GROUP PLLC P. O. BOX 270 FREDERICKSBURG, VA 22404				
EXAMINER				
RIYAMI, ABDULLA A				
ART UNIT		PAPER NUMBER		
2416				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Response to Arguments

Applicant's arguments filed 07/20/2009 have been fully considered but they are not persuasive. Applicant argues that the prior art fails to disclose (1) storing only data portions in locations in a first memory; (2) storing only record portions in a second memory having fixed size memory locations equal in size to the size of the record portions; and (3) the memory locations in the first memory being (i) in blocks of different sizes and (ii) allocated to the data portions according to the size of the data portions.

Examiner respectfully disagrees with Applicant's characterization of the prior art.

Mittal does disclose storing only data portions in locations in a first memory (see figure 2, ingress memory 20, see column 4, lines 31-40, the ingress memory hub writes the packet into ingress memory according to the ingress flow id). The **data packets have data portions** so as is mentioned in column 2, lines 25-29, the ingress memory hub receives **packets** from the source port and stores the **packets** in ingress memory.

Mittal does disclose storing only record portions in a second memory having fixed size memory locations equal in size to the size of the record portions (see figure 2, ingress memory hub 18, ingress queues 46 or ingress queues 42, see column 4, lines 5-30, each ingress queue 46 is associated with flow id, length and class of service, each ingress queue 42 includes field 43 that tracks the total number of packets for flow, also includes ordered queue that identifies length of each packet for that particular flow id in the order the packets are received). Notice in column 4, lines 10-12, the header identifies the ingress flow id and the **length** for the packet. Notice in lines 25-30, each

ingress queue includes an ordered queue that identifies **the length of each packet** (record portion) received.

Mittal does disclose the memory locations in the first memory being (i) in blocks of different sizes (see figure 5a, there are three packets, packet A and B have size L whereas packet C has size 2L) and (ii) allocated to the data portions according to the size of the data portions. (see figure 2, ingress memory 20, see column 4, lines 31-40, the ingress memory hub writes the packet into ingress memory according to the ingress flow id, see figure 2, ingress memory hub 18, ingress queues 46 or ingress queues 42, see column 4, lines 5-30, each ingress queue 46 is associated with flow id, length and class of service, each ingress queue 42 includes field 43 that tracks the total number of packets for flow, also includes ordered queue that identifies length of each packet for that particular flow id in the order the packets are received). Notice in figure 5a, there are three packets, packet A and B have **size L**, whereas packet C has **size 2L** and are all stored in the ingress memory also notice in column 4, lines 65-66, length of each packet is received, thus the memory stores packets of **different sizes**.

There has been no distinction between the data portion and record portion in the claim. It is important to note that data portion and record portion as mentioned in the claims is not the same as header and payload as is well known in the art, and are interpreted as portions of data, i.e. a record portion can be from a payload or a header, a data portion can be from a header or payload or both.

Art Unit: 2416

Provisional application from which Radharkrishnan (U.S. Patent Publication No. 2004/0022094) claims priority should be requested by Applicant for review purposes or access the PAIR database.

/Aung S. Moe/

Supervisory Patent Examiner, Art Unit 2416